REMARKS

Claims 1-21 are pending in the present application. In the above amendments, claims 3 and 8 have been amended.

In the Office Action mailed April 6, 2005, the Examiner rejected claims 5-6 under 35 U.S.C. §112, as failing to comply with the enablement requirement. The Examiner rejected claims 1, 2, 3, 12, 16, 17, 20, and 21 under 35 U.S.C. §102(e) as being anticipated by US Pub. 2003/0076801 by Aikawa et al. (hereinafter "Aikawa"). The Examiner rejected claims 4, 14, and 19 under 35 U.S.C. §103(a) as being unpatentable over Aikawa in view of US Pub. 2004/0100935 by Papageorngiou et al. (hereinafter "Papageorngiou"). The Examiner rejected claims 7 and 18 as being unpatentable over Aikawa in view of Papageorngiou and US Pub. 2003/0086512 by Rick et al. (hereinafter "Rick"). The Examiner rejected claim 17 as being unpatentable over Aikawa in view of US Patent 6,711,219 by Thomas et al. (hereinafter "Thomas").

Claims 8-11, 13, and 15 are objected to, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicants respectfully respond to this Office Action.

Claim 3 has been amended to remove a grammatical error, and does not alter the scope of the claim as originally filed.

Claim 8 has been amended to depend on claim 2, providing antecedent basis for the memory.

35 U.S.C. §112

The Examiner rejects claims 5 and 6 as failing to comply with the enablement requirement. The Examiner asserts that the claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. Applicants respectfully disagree, and provide examples from the specification as filed to support each limitation of these claims. Claims 5 and 6 are included in the application as

filed, and therefore are included in the specification. Additional support may be found as follows: The processor is identified in precedent claims, and is supported in the specification in various places, including processor 250 in paragraph [1040]. The terms "adds", "integer" and "multiple" are well known in mathematics, and would thus be readily available to one skilled in the relevant art. Chips and slots are well known in the art, and examples are described in the W-CDMA standard cited in the specification, as well as myriad other references known in the art. An integer multiple of the number of chips would be well understood by one of skill in the art, as would adding an integer multiple of a number of chips to a search result. Regarding claim 5, an example embodiment supporting search results and comparing of search results is described in [1050], among others. Regarding claim 6, example embodiments supporting stored offsets are described in [1008] and [1065]. Thus, given the application as filed, one skilled in the art would be enabled to make and practice the invention. As such, the rejection of claims 5 and 6 should be withdrawn.

35 U.S.C. §102

The standard for anticipation under §102 requires "the presence in a single prior art disclosure of all elements of a claimed invention arranged as in that claim." Carella v. Starlight Archery & Pro Line Co., 804 F.2d 135, 138, 231 U.S.P.Q.D (BNA) 644, 646 (Fed. Cir. 1998) (*quoting Panduit Corp. v. Dennison Mfg. Co.*, 774 F.2d 1082, 1101, 227 U.S.P.Q. (BNA) 337, 350 (Fed. Cir. 1985)) (*additional citations omitted*). As discussed further below, the Examiner has failed to identify each and every claim limitation, and has therefore failed to set forth a prima facie case for anticipation as required by §102.

With respect to claims 1, 16, 20, and 21, the Examiner asserts that Aikawa teaches "a cell search controller that correlates a received signal with a synchronization sequence to produce a first plurality of search results wherein each search result comprises at least one of an energy indicator or an offset ... and a processor for comparing the stored offset with the search result offset and deleting the corresponding search results from the first plurality of search results when the search result offset is within a predetermined threshold of the stored offset ...". Applicants respectfully disagree with the Examiner's characterization of Aikawa. Aikawa teaches of extracting maximum correlation paths from detected paths during acquisition, and removing

multipath components around the extracted maximum correlation paths. Nowhere does Aikawa teach of storing offsets, or of comparing a stored offset with a search result, or removing a corresponding search result from a plurality of search results when the search result is within a pre-determined threshold of the stored offset. Thus, Aikawa does not teach each of the limitations of claims 1, 16, 20, or 21.

With respect to dependent claims 2, 3, 12, and 17, the Examiner has failed to set forth a prima facie case for anticipation for the respective parent claims, and therefore for the dependent claims as well. Furthermore, the Examiner has also failed to point out where Aikawa teaches the limitations of various dependent claims.

With respect to claim 2, the Examiner cites Fig. 4 and Page 5, par. 55, and asserts that Aikawa teaches "a plurality of scrambling code identifiers wherein the scrambling code identifiers are responsive to the multi-path deletion section 24 in which contains the predetermined offset table". The Examiner also asserts that "one of ordinary skill in the art would clearly recognize that it is well known in the art to store the scrambling code identifiers responsive to the predetermined offset in a memory. First, Applicants point out that to support a case for anticipation (see above), the single prior art reference, Aikawa, must teach all elements of a claimed invention arranged as in that claim. What is "well known in the art" but not disclosed in Aikawa is irrelevant for purposes of anticipation. Thus, the Examiner's argument is not a proper basis for a §102 rejection. Second, the cited portions do not teach a memory, or a plurality of scrambling code identifiers, or a predetermined offset table. Thus, the Examiner has mischaracterized Aikawa, in that it does not teach what the Examiner purports that it teaches. Third, the Examiner's characterization of Aikawa does not recite the limitations of claim 2. The Examiner has failed to assert that Aikawa teaches a memory for storing a first plurality of scrambling code identifiers and associated offsets, the stored offset selected therefrom. Any one of these three arguments would be sufficient to overcome the Examiner's rejection based on anticipation. Given that all three hold true, as well as the arguments with respect to the parent claim, the Examiner's rejection should be withdrawn.

With respect to claim 12, the fixed threshold cited in Aikawa is not applicable to removing the corresponding search result from the first plurality of search results when the

search result offset is within a pre-determined threshold of the stored offset, as described above with respect to claim 1.

35 U.S.C. §103

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation of, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all the claim limitations.

For each §103(a) rejection in this Office Action, Applicants submit: the prior art of record does not provide a suggestion or motivation to modify the reference; there is not a reasonable expectation of success, and the reference does not teach or suggest all the claim limitations.

Each of the Examiner's rejections use Aikawa as the basis for teaching one or more claimed elements. The arguments detailed above regarding Aikawa thus apply to each of these rejections as well. Thus, the prima facie case of obviousness is not made, as all of the claim limitations are not taught nor suggested. Therefore, the rejections to claims 4, 7, 14, 17, 18, and 19 should be withdrawn.

Furthermore, the Examiner has failed to point out where the suggestion or motivation to combine the references is given. With respect to Papageorgiou and Rick, the Examiner states categorically that "it would have been obvious to one of ordinary skill in the art to combine the teaching" of the references. The Examiner is silent as to the suggestion or motivation to combine Thomas with Aikawa. If the Examiner is relying on personal knowledge to support each finding of what is known in the art, including which documents to combine and how to do so, Applicants request that Examiner provide an affidavit or declaration setting forth specific factual statements and explanation to support the finding per 37 CFR 1.104(d)(2). Thus, the prima facie case of obviousness fails for lacking a suggestion to modify or combine reference teachings, and the rejections to claims 4, 7, 14, 17, 18, and 19 should be withdrawn for this reason as well.

With respect to claim 4, the Examiner asserts the combination would "establish slot synchronization". Again, Applicants point out that the combination fails to teach or suggest each claim limitation. Furthermore, the Examiner's conclusion of the combined teaching, "slot

synchronization" is not a recited element of claim 4, and so the Examiner's conclusion is not relevant to an obviousness rejection of the claim. Similar arguments apply with respect to claims 14 and 19.

With respect to claims 7 and 18, the Examiner now requires three references: Aikawa, Papageorngiou and Rick. As described above, the combination fails to recite each claim limitation, and there is no suggestion to combine two references, let alone three. Furthermore, the Examiner cites Rick as teaching "ray classification", but fails to point out how that is relevant to the limitations recited in these claims.

With respect to claim 17, the arguments described above continue to apply. Furthermore, the Examiner concedes that Aikawa does not teach selecting the stored offset from a plurality of scrambling code identifiers and associated offsets stored in a memory. The Examiner does not state that Thomas teaches this limitation either. The Examiner simply points out that Thomas defines the term "code offset", as cited. Note that "code offset" is not a recited limitation of claim 17, nor does the Examiner point out how it is relevant to the limitations of the claim. Neither does Thomas teach of storing a code offset in a memory, nor of storing a plurality of scrambling code identifiers and associated offsets stored in a memory, nor of selecting a stored offset therefrom. In fact, Thomas does not use the term memory in any way.

Thus, for these reasons, as well as additional arguments (not included herein), a prima facie case of obviousness has not been made, and the associated rejections should be withdrawn.

Specification

Applicant provides herewith amendments to the specification. The amendments to the specification are made by presenting marked up replacement paragraphs which identify changes made relative to the immediate prior version.

A replacement paragraph [1041] is provided which includes the citation to the copending US Patent Application No., per the Examiner's request.

Applicant believes these changes add no new matter to the application and are fully supported by the original disclosure.

REQUEST FOR ALLOWANCE

In view of the foregoing, Applicant submits that all pending claims in the application are patentable. Accordingly, reconsideration and allowance of this application is earnestly solicited. Should any issues remain unresolved, the Examiner is encouraged to telephone the undersigned at the number provided below.

Respectfully submitted,

Dated: July 6, 2005

By: _____
George C. Pappas, Reg. No. 35,065
Tel: (858) 651-1306

QUALCOMM Incorporated
5775 Morehouse Drive
San Diego, California 92121
Telephone: (858) 651-4125
Facsimile: (858) 658-2502

/BY
KENYON JENCKES
REG. NO. 41,873